**In the Claims**

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Currently amended) A bandgap reference voltage circuit configured to reduce the Early effect, the circuit including a first amplifier having first and second inputs and providing a buffered voltage reference at the output thereof, the amplifier being coupled at its first input to a first bipolar transistor and at the second input to a second bipolar transistor, the second transistor having an emitter area larger than that of the first transistor, and wherein:

the second transistor is coupled at its emitter to a load resistor, the load resistor providing, in use, a measure of the difference in base emitter voltages between the first and second transistors, $\Delta Vbe$, for use in the formation of the bandgap reference voltage,

the bases of each transistor are commonly coupled such that the base of the first and second transistor is at the same potential,

one of the first and second transistors is provided in a diode connected configuration, and

the base collector voltage of the other of the first and second transistors is maintained at zero by the amplifier which is coupled in a feedback loop to the collector of each of the transistors, and

the circuit further includes a third transistor and a fourth transistor, the third transistor being coupled to the emitter of the first transistor and the fourth transistor being coupled via the load resistor to the emitter of the second transistor, the emitter area of the fourth transistor being greater than that of the first or third transistor, such that the first and third transistors operate at a higher current density than the second and fourth transistors and wherein a PTAT voltage is provided via a resistor, in the feedback loop, at the second input to the amplifier such that the voltage provided at the output of the amplifier is a combination of the base-emitter voltages of the first and third transistors plus the PTAT voltage.

2. (Cancelled)

3. (Currently amended) The circuit as claimed in claim [[2]]1 wherein each of the third and fourth transistors are provided in a diode connected configuration.

4. (Currently amended) The circuit as claimed in claim [[2]]1 wherein the emitter of the third transistor is coupled via a second resistor to ground, the value of the resistor effecting a shifting of the reference voltage from twice the natural bandgap voltage to a desired voltage, thereby enabling an offset adjustment to the circuit.

5. (Original) The circuit as claimed in claim 3 further including a third and fourth resistor provided in each of the feedback loop paths between the output of the amplifier and the collectors of the first and second transistors respectively.

6. (Original) The circuit as claimed in claim 5 wherein the resistors provided in each of the feedback loops are substantially the same value.

7. (Original) The circuit as claimed in claim 5 wherein the resistors provided in each of the feedback loops are of different values.

8. (Original) The circuit as claimed in claim 5 further including circuitry adapted to provide the base current for the non-diode connected transistor and to extract that same current from the collector of the same transistor, thereby maintaining the collector current of each of the first and second transistors at the same value.

9. (Previously presented) The circuit as claimed in claim 5 further including circuitry adapted to provide the base current for the non-diode connected transistor and to extract that same current from the collector of the same transistor, the circuitry adapted to compensate for base current variation between the non-diode connected transistor and the other transistor, thereby reducing errors in the circuit due to the base current of bipolar transistors.

10. (Original) The circuit as claimed in claim 8 wherein the non-diode connected transistor is the first transistor and the circuitry adapted to extract the current from the collector of the first transistor includes a replication of the leg of the circuit defined by the first and third transistors, the replicated leg including a fifth and sixth transistor of the circuit, the base of the fifth transistor being coupled to the collector of the first transistor, the emitter of the fifth transistor being coupled to the collector of the sixth transistor, the base of the sixth transistor being coupled to the diode connected base of the third transistor thereby providing a current mirror, such that a base current is extracted from the collector of the first transistor by the fifth transistor.

11. (Previously presented) The circuit as claimed in claim 10 wherein the base current of the first and second transistors is further mirrored via seventh and eight transistors and a current mirror, the base currents of the sixth and eight transistors being supplied by a double current mirror from the output of the amplifier and the base current of the first and second transistors being supplied by another double current mirror such that the collector currents of each of the first, second, third, sixth and eight transistors are the same.

12. (Original) The circuit as claimed in claim 11 wherein the collector of the fifth transistor is coupled via a resistor to the output of the amplifier, the value of the resistor being substantially equivalent to that of the fourth resistor such that the base current of the fifth transistor tracks the base current of the first transistor.

13. (Original) The circuit as claimed in claim 11 wherein the base current of the first and second transistors is further mirrored via a series of mirrors coupled to the fifth and seventh transistors such that the mirrored current may be extracted from the emitters of the fifth and seventh transistors thereby ensuring that the collector currents of the fifth and seventh transistors are substantially the same value, this current being further mirrored via a current mirror coupled between the collector of the seventh transistor and the output of the amplifier, thereby providing a PTAT current.

14. (Original) The circuit as claimed in claim 3 further including circuitry adapted to provide a correction voltage adapted to compensate for the curvature of the voltage of the first and third transistors, the incorporation of the correction voltage effecting a cancelling of the curvature.

15. (Previously presented) The circuit as claimed in claim 14 wherein the circuitry adapted to provide a correction voltage is adapted to provide a mixture of PTAT and CTAT current into the fourth transistor.

16. (Previously presented) The circuit as claimed in claim 14 wherein the correction voltage is provided by mirroring the base-emitter voltage of the fourth transistor across a resistor and effecting the generation of a complimentary to absolute temperature (CTAT) current using current mirrors and amplifier, the CTAT current being provided back into the fourth transistor via at least one current mirror thereby replicating across the first resistor a voltage having an inverse curvature, the combination of this replicated voltage and the previously present voltage ($\Delta V_{be}$) effecting a cancellation of the curvature.

17. (Original) The circuit as claimed in claim 15 wherein the size of the voltage having an inverse curvature may be modified by changing the slope of the current provided by the current mirror and fourth transistor.

18. (Currently amended) The circuit as claimed in claim [[2]]1 further including a plurality of additional transistors coupled to the third and fourth transistors, the plurality of additional transistors being provided in a stack arrangement, thereby enabling a use of the reference circuit with higher reference voltages.

19. (Previously presented) A bandgap reference voltage circuit configured to reduce the Early effect, the circuit including a first amplifier having first and second inputs and providing a voltage reference at the output thereof, the amplifier being coupled at its first input to a first transistor and at the second input to a second transistor, the amplifier being coupled in a feedback loop to the collector of each of the transistors, the second transistor having an emitter

area larger than that of the first transistor, the circuit additionally including a third and fourth transistor, each being provided in a diode connected configuration, and wherein:

the second transistor is coupled at its emitter to a load resistor, the load resistor providing, in use, a measure of the difference in base emitter voltages between the first and second transistors, $\Delta Vbe$, for use in the formation of the bandgap reference voltage,

the bases of each transistor are commonly coupled such that the base of the first and second transistor is at the same potential,

one of the first and second transistors is provided in a diode connected configuration,

the third transistor is coupled to the emitter of the first transistor and the fourth transistor is coupled via the load resistor to the emitter of the second transistor, the emitter area of the fourth transistor being greater than that of the first or third transistor, such that the first and third transistors operate at a higher current density than the second and fourth transistors and wherein a PTAT voltage is provided via a resistor, in a feedback loop of the amplifier, at the second input to the amplifier such that the voltage provided at the output of the amplifier is a combination of the base emitter voltages of the first and third transistors plus the PTAT voltage, and

the base-collector voltage of the other of the first and second transistors is minimized by the amplifier which is coupled in a feedback loop to the collector of each of the transistors.

20. (Currently amended) A method of providing a bandgap reference voltage circuit configured to compensate for the Early effect, the method comprising the acts of:

providing first and second transistors, each transistor adapted to operate at different current densities, the first transistor being provided in a diode connected configuration, the transistors being additionally coupled to the inputs of an amplifier,

<u>providing third and fourth transistors, the third transistor being coupled to the emitter of the first transistor and the fourth transistor being coupled via a load resistor to the emitter of the second transistor, the emitter area of the fourth transistor being greater than that of the first or third transistor, such that the first and third transistors operate at a higher current density than the second and forth transistors,</u>

scaling the voltage difference between two transistors operating at different current densities so as to provide a reference voltage at an output of the amplifier, and

providing a feedback loop, the feedback loop coupling each of the first and second transistors to the output of the amplifier so as to provide at an output of an amplifier a buffered voltage reference, such that the collector base voltage of each of the first and second transistors is reduced to zero, and further wherein a PTAT voltage is provided via a resistor, in the feedback loop, at the second input to the amplifier such that the voltage provided at the output of the amplifier is a combination of the base emitter voltages of the first and third transistors plus the PTAT voltage.